CLAIMS

What is claimed is:

1. A method for initializing a lockstep mode test case simulation of a multi-core processor design, comprising the steps of:

determining one or more initialization statements of the test case simulation that identify one or more first registers of a simulated primary core;

if the test case simulation specifies that the multi-core processor design operates in lockstep mode, modifying scope of the initialization statements;

initializing the first registers specified by the initialization statements; and

processing unmodified initialization statements to initialize second registers of simulated cores of the multi-core processor design, as specified by the unmodified initialization statements.

2. The method of claim 1, the test case simulation comprising one or more test cases.

3. The method of claim 1, wherein the step of initializing comprises loading values from the modified initialization statements into the first registers.

4. The method of claim 1, wherein the step of processing comprises loading values from the unmodified initialization statements into the second registers.

5. The method of claim 1, the step of modifying comprising undesignating the simulated primary core.

6. The method of claim 1, further comprising writing a randomly selected value to non-initialized matching registers of each simulated core.

7. A system for initializing a lockstep mode test case simulation of a multi-core processor design, comprising:

means for determining one or more initialization statements of the test case simulation that identify one or more first registers of a simulated primary core;

means for modifying scope of the initialization statements when the test case simulation specifies that the multi-core processor design operates in lockstep mode;

means for initializing the first registers specified by the initialization statements; and

means for processing unmodified initialization statements to initialize second registers of simulated cores of the multi-core processor design, as specified by the unmodified initialization statements.

8. The system of claim 7, the test case simulation comprising one or more test cases.

9. The system of claim 7, wherein the means for initializing comprises means for loading values from the modified initialization statements into the first registers.

10. The system of claim 7, wherein the means for processing comprises means for loading values from the unmodified initialization statements into the second registers.

11. The system of claim 7, wherein the means for modifying comprising means for undesignating the simulated primary core.

12. The method of claim 7, further comprising means for writing a randomly selected value to non-initialized matching registers of each simulated core.

13. A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for initializing a lockstep mode test case simulation of a multi-core processor design, comprising:

instructions for determining one or more initialization statements of the test case simulation that identify one or more first registers of a simulated primary core;

instructions for modifying scope of the initialization statements when the test case simulation specifies that the multi-core processor design operates in lockstep mode;

instructions for initializing the first registers specified by the initialization statements; and

instructions for processing unmodified initialization statements to initialize second registers of simulated cores of the multi-core processor design, as specified by the unmodified initialization statements.

14. The software product of claim 13, the test case simulation comprising one or more test cases.

15. The software product of claim 13, wherein the instructions for initializing comprises instructions for loading values from the modified initialization statements into the first registers.

16. The software product of claim 13, wherein the instructions for processing comprises instructions for loading values from the unmodified initialization statements into the second registers.

17. The software product of claim 13, wherein the instructions for modifying comprising instructions for undesignating the simulated primary core.

18. The software product of claim 13, further comprising instructions for writing a randomly selected value to non-initialized matching registers of each simulated core.

19. A system for initializing a lockstep mode test case simulation of a multi-core processor design, comprising:

a simulated multi-core processor design with a simulated primary core and one or more other simulated cores; and

a test case with one or more primary core initialization statements;

a lockstep core initializer for processing the initialization statements to identify one or more first registers of the simulated primary core, wherein if the lockstep core initializer determines that the test case

simulation specifies that the multi-core processor design operates in lockstep mode, the lockstep core initializer (a) modifies scope of the initialization statements, (b) initializes the first registers specified by the initialization statements, and (c) processes unmodified initialization statements to initialize second registers of simulated cores of the multi-core processor design.